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TITLE: TESTING SYSTEM OF SEMICONDUCTOR LOGIC CIRCUIT

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ABSTRACT:

PURPOSE: To generate a practical test vector amount automatically, by extracting a network structure of a logic circuit from a logic circuit description language.

CONSTITUTION: A network structure of a logic circuit is extracted from a logic circuit description language of a register transfer level, and subsequently nodes of the network structure and relationships in connection between the nodes are weighted. Then, the connection relationship is selected in accordance with the weight and a test vector satisfying a condition for selection of the connection relationship is generated automatically. The test vector includes an explanatory description as to what part of the logic circuit description be tested. In addition, an editing function of the generated test vector is provided. By using this editing function, it is possible to combine test steps for tests, including a test of an input circuit, a test of an output circuit, a test of an internal data bus and a test of an arithmetic processing.

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